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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,274	10/09/2003	Yoshikazu Ohara	4074-8	5972

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,274	OHARA, YOSHIKAZU	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 26-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-6 and 13* is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/27/2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 27-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 27-30 all require "that areas of the semiconductor chip where no groove is formed are not flexible." There is no part of the specification as filed that discloses that element-forming regions (which are the claimed parts of the chip where no groove is formed) are not flexible. In fact the specification as filed discloses a device where only the opposite is true. Paragraph 0056 of the specification as filed states that "semiconductor chip T1 as a whole becomes flexible." Paragraph 0092 reiterates "the semiconductor device module M as a whole can be flexibly curved."

Addressing specifically the flexibility of the element forming regions, paragraph 0012 states that when bending stress is applied to the semiconductor device, the element forming regions are curved ("hardly curved," but nonetheless curved). Curving in response to bending stress is the definition of flexibility.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by OKADA (5,531,002).

Okada discloses a semiconductor device with a flexible semiconductor chip including an element forming region 911 where a semiconductor element 955 is formed and an element non-forming region 912-913 where no semiconductor element 955 is formed, each of the element forming region 911 and the element non-forming region 912-913 being provided on a front surface of a silicon substrate 910, a plurality of grooves (no part #, seen under a portion 912 of the element non-forming region 912-913), formed parallel to each other and having a wider width in an opening portion than in a bottom portion, formed in a portion of a rear surface of said silicon substrate 910

corresponding to said element non-forming region 912-913, wherein said groove does not extend all the way through the silicon substrate 910, so that the **region of the semiconductor chip that corresponds to the portion where the groove is formed is flexible**, and wherein the groove is not provided under any portion of the element forming region 911, and wherein no part of the grooves (recall that the grooves have no part #s, they are seen under a portion 912 of the element non-forming region 912-913) extends all the way through the silicon substrate. Note figures 40-42 and column 27 lines 11-46 of Okada.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002).

Okada discloses a semiconductor device with every limitation of claims 10 and 11 except that a material softer than the silicon substrate fills the grooves and coats the rear surface of said silicon substrate. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, a second embodiment disclosed by Okada discloses a semiconductor device with silicon oil (a material softer than silicon) filling grooves 201 and coating the rear surface of a silicon substrate 200. Note figures 32A-C and 33 and column 25 lines 1-5 of Okada. Therefore, it would have been obvious to a person having skill in the art to augment Okada's semiconductor device with the silicon oil filling the grooves and coating the rear surface of said silicon substrate, such as taught by Okada's second embodiment in order to provide impact or vibration absorbing effect to thus provide improved impact and vibration resistance.

B. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002) in view of KNECHT ET AL. (4,905,575).

Okada discloses a semiconductor device with every limitation of claims 7 and 9 except that the groove has a substantially uniform width from a bottom portion to an opening portion of said groove, as recited in claim 7, or wherein said groove has a bottom portion with a curved surface, as recited in claim 9. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, with regard to claim 7, Knecht et al. discloses a semiconductor device 70 having an element forming region 71 where a semiconductor element is formed and an element non-forming region 76 where no semiconductor element is formed, on a front surface of a silicon substrate 72, comprising a plurality of grooves 75 each having substantially uniform width from a bottom portion to an opening portion of that groove

75. Note figure 6 of Knecht et al. Further, with regard to claim 9, Knecht et al. discloses a semiconductor device 90 having an element forming region 94 where a semiconductor element 91 is formed and an element non-forming region 97 where no semiconductor element formed, on a front surface of a silicon substrate 92, comprising a plurality of grooves 95 having bottom portions with curved surfaces. Note figure 8 of Knecht et al. Therefore, it would have been obvious to a person having skill in the art to augment of Okada's semiconductor device with the groove having a substantially uniform width from a bottom portion to an opening portion of said groove, or the groove having a bottom portion with a curved surface, such as taught by Knecht et al. in order to provide a different clearance between parts of the silicon substrate to thus optimize flexibility according to need.

C. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002) in view of WILLIS ET AL. (5,912,427).

Okada discloses a semiconductor device with every limitation of claim 12 except that a plurality of said element forming regions are isolated from each other, and said element non-forming region is a region sandwiched between said element forming regions. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, Willis et al. discloses a semiconductor device 500 having silicon substrate 501 coating the rear surface of said silicon substrate 501; a plurality of element forming regions 580 isolated from each other, where semiconductor elements are formed; and an element non-forming region 510, sandwiched between said element forming regions

580, where a semiconductor element is not formed, on a front surface of said silicon substrate 501, said semiconductor device 500 comprising a groove 503 formed in a portion of a rear surface of said substrate 501 corresponding to said element non-forming region 510. Note figure 12 and column 9 lines 1-15 of Willis et al. Therefore, it would have been obvious to a person having skill in the art to augment of Okada's semiconductor device with the plurality of said element forming regions, isolated from each other, wherein said element non-forming region is a region sandwiched between said element forming regions, such as taught by Willis et al. in order to increase the number of element forming region and thus the number of elements, to thus provide increased functionality.

Response to Arguments

5. Applicant's arguments filed 10/27/2005 have been fully considered but they are not persuasive.

It is argued, at page 7 of the remarks, that "Okada at col. 9, lines 40-41 and col. 12, lines 41-42, explains that the entire substrate is flexible." However, if the entire substrate is flexible, it follows that each individual region of the substrate is flexible, including **the region of the semiconductor chip that corresponds to the portion where the groove is formed**. Applicant's argument is therefore an admission on Applicant's part that the region of the semiconductor chip that corresponds to the

portion where the groove is formed is flexible, as required by amended claims 1 and 8-10.

It is further argued, at page 7 of the remarks, that "Moreover, claim 27 requires that the region of the semiconductor chip that corresponds to the portion where the groove is formed is flexible, so that areas of the semiconductor chip where no groove is formed are not flexible." However, as explained above, there is no support in the application as filed for a claim that any part of the semiconductor chip is not flexible. Therefore claims 27-30 fail to meet the written description requirement of §112 ¶1.

It is argued, at page 8 of the remarks, that "Okada teaches [that] all of holes 961-964 ... extend all the way through the substrate [and] much of the alleged grooves extend all the way through the alleged substrate." However, in the first instance, a hole is not a groove, so properties of Okada's holes are irrelevant. Note, figure 41, that holes 961-964 are formed between element non-forming regions 912, while grooves (seen in cross sectional figure 40 without part #s) are formed, as the claims require, under element non-forming regions 912. Secondly, for the alleged fact that much of the grooves extend all the way through the substrate to be relevant applicant's claims would have to limit the amount of the claimed grooves that is allowed to extend all the way through the substrate. Applicant's claims 1 and 8-10 each claim simply that "said groove does not extend all the way through the silicon substrate." In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., limits on how much or how little of said

grooves extend all the way through the silicon substrate) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Allowable Subject Matter

6. Claims 4-6 and 13 are allowable are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device having an element forming region where a semiconductor element is formed and an element non-forming region where a semiconductor element is not formed, on a front surface of a silicon substrate, comprising a groove formed in a portion of a rear surface of said substrate corresponding to said element non-forming region, wherein said grooves are formed to extend in directions crossing each other, as recited in claim 4, or said semiconductor device, bonded to a curved bonding substrate, as recited in claim 13.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

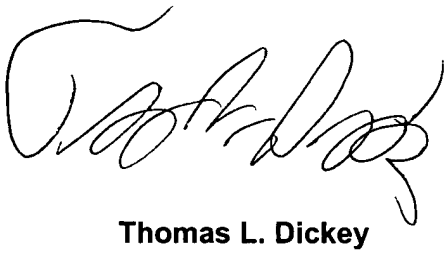
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
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Art Unit 2826
12/05